Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (cancelled).

Claim 2 (currently amended): A semiconductor memory device comprising:

a semiconductor substrate;

a dielectric gate stack **comprising at least a first layer and a second layer** formed on a channel region of the substrate, **the first and second layer each formed of a material selected from among silicon carbide, silicon oxynitride, silicon nitride, and amorphous silicon nitride** ~~the dielectric gate stack having a top portion and a bottom portion~~; **and**

~~the dielectric gate stack including~~ an electron trapping layer **arranged between and in contact with the first and second layers of the stack, the electron trapping layer consists of an electron trapping material** ~~of an electron trapping~~ **is** selected from ~~among the group consisting of~~ zirconium oxide and aluminum oxide.

Claim 3 (withdrawn). The semiconductor memory device of Claim 2 wherein the dielectric gate stack is comprised entirely of the electron trapping layer.

Claim 4 (cancelled).

Claim 5 (currently amended): The semiconductor memory device of Claim **2** **[[4]]** wherein the first layer of dielectric material and the second layer of dielectric material are each comprised of silicon **nitride** ~~dioxide~~.

Claim 6 (cancelled).

Claim 7 (withdrawn). The semiconductor memory device of Claim 1 wherein the dielectric gate stack is comprised entirely of the electron trapping layer that comprises zirconium oxide and wherein an interface between the electron trapping layer and the channel region of the substrate comprises $Zr_xSi_yO_z$.

Claim 8 (withdrawn). The semiconductor memory device of Claim 1 wherein the dielectric gate region is comprised entirely of the electron trapping layer that comprises aluminum oxide and wherein an interface between the electron trapping layer and the channel region of the substrate comprises $Al_xSi_yO_z$.

Claim 9 (withdrawn). The semiconductor memory device of Claim 1 wherein the dielectric gate region is comprised entirely of the electron trapping layer that comprises hafnium oxide and wherein an interface between the electron trapping layer and the channel region of the substrate comprises $Hf_xSi_yO_z$.

Claim 10 (previously presented): A semiconductor integrated circuit having the memory devices of Claim 2 formed thereon.

Claim 11 (cancelled).

Claim 12 (withdrawn): A method for forming a memory device comprising:

providing a semiconductor substrate;

forming a gate stack over a channel region of the substrate such that the gate stack includes a layer of electron trapping material; and

forming a gate electrode connected with a top portion of the gate stack.

Claim 13 (withdrawn): The method for forming a memory device as in Claim 12, wherein forming the layer of electron trapping material comprises formed the layer of electron trapping material with a material selected from among the group consisting of zirconium oxide, hafnium oxide, and aluminum oxide.

Claim 14 (withdrawn): The method for forming a memory device as in Claim 12 wherein forming the gate stack comprises forming a first layer of dielectric material over the channel

region of the substrate and forming the layer of electron trapping material over the first layer of dielectric material and forming a gate electrode connected with the layer of electron trapping material.

Claim 15 (withdrawn): The method for forming a memory device as in Claim 14, wherein forming the layer of electron trapping material comprises formed the layer of electron trapping material with a material selected from among the group consisting of zirconium oxide, hafnium oxide, and aluminum oxide.

Claim 16 (withdrawn): The method for forming a memory device as in Claim 15, wherein forming the first layer of dielectric material comprises formed the first layer of dielectric material with a silicon oxide material.

Claim 17 (withdrawn): The method for forming a memory device as in Claim 12 wherein forming the gate stack comprises:

forming a first layer of dielectric material over the channel region of the substrate;

forming the layer of electron trapping material over the first layer of dielectric material;

forming a second layer of dielectric material over the layer of electron trapping material; and

forming a gate electrode connected with a top portion of the second layer of dielectric material.

Claim 18 (withdrawn): A method for forming a memory device as in Claim 17, wherein forming the layer of electron trapping material comprises formed the layer of electron trapping material with a material selected from among the group consisting of zirconium oxide, hafnium oxide, and aluminum oxide.

Claim 19 (withdrawn): The method for forming a memory device as in Claim 18, wherein forming the first layer of dielectric material and forming the second layer of dielectric material comprises formed the first layer of dielectric material and the second layer of dielectric material with a silicon oxide material.

Claim 20 (withdrawn): The method for forming a memory device as in Claim 18, wherein forming the first layer of dielectric material and forming the second layer of dielectric material comprises formed the first layer of dielectric material and the second layer of dielectric material with different dielectric material.

Claim 21 (new). The semiconductor memory device of Claim 2 wherein the electron trapping material consists of zirconium oxide.

Claim 22 (new). The semiconductor memory device of Claim 2 wherein the electron trapping material consists of aluminum oxide.

Claim 23 (new). The semiconductor memory device of Claim 2 wherein the first layer of the gate stack and the second layer of the gate stack each consist of amorphous silicon nitride.

Claim 24 (new). The semiconductor memory device of Claim 2 wherein the first layer of the gate stack includes silicon nitride.

Claim 25 (new). The semiconductor memory device of Claim 24 wherein the first layer of the gate stack includes amorphous silicon nitride.

Claim 26 (new). The semiconductor memory device of Claim 2 wherein the first layer of the gate stack includes silicon oxynitride.

Claim 27 (new). The semiconductor memory device of Claim 2 wherein the first layer of the gate stack includes silicon carbide.

Claim 28 (new). The semiconductor memory device of Claim 24 wherein the second layer of the gate stack is formed of a different material than the first layer of gate stack.

Claim 29 (new). The semiconductor memory device of Claim 25 wherein the second layer of the gate stack is formed of a different material than the first layer of gate stack.

Claim 30 (new). The semiconductor memory device of Claim 26 wherein the second layer of the gate stack is formed of a different material than the first layer of gate stack.

Claim 31 (new). The semiconductor memory device of Claim 27 wherein the second layer of the gate stack is formed of a different material than the first layer of gate stack.